ALPHA DATA

XRM2-ADC-S4/3G User Manual

Document Revision: 1.2
16th Feb 2016

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1 Introduction

Figure 1 : XRM2-ADC-S4/3G

The XRM2-ADC-S4/3G is a front panel adapter card designed principally for use with Alpha Data's ADM-XRC4 and ADM-XRC5 FPGA-based PMC cards, although some limited functionality is possible with the ADM-XP PMC card.

The XRM2-ADC-S4/3G is based on the ADC083000 from National Semiconductor and provides a single channel of analogue to digital conversion with 8 bit resolution at sampling rates up to 3.0 GHz It is aimed at applications such as IF signal sampling.

An external clock source may be used or an internally generated clock can be used to provide the sampling clock.

An auxiliary I/O port is provided for use as a trigger input and general purpose signalling. An additional two ports are available for use as high-speed interconnect between boards for synchronisation.

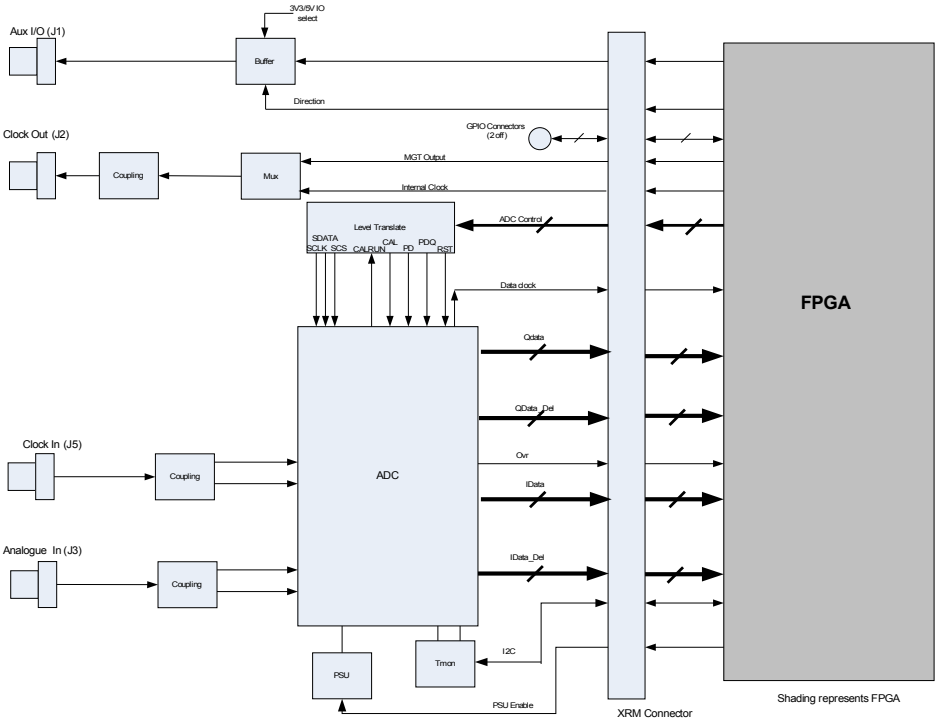

Figure 2 : XRM Block Diagram

2 Installation

The XRM2-ADC-S4/3G is designed to plug in to the front panel connector (SAMTEC QSH series) on the XRC series of cards. The retaining screws should be tightened to secure the XRM2-ADC-S4/3G.

Note:
This operation should not be performed while the PMC card is powered up.

2.1 Handling instructions

Observe precautions for preventing damage to components by electrostatic discharge. Personnel handling the board should take SSD precautions.

2.1.1 Handling Instructions

The components on this board can be damaged by electrostatic discharge (ESD). To prevent damage, observe SSD precautions:

- Always wear a wrist-strap when handling the card
- Hold the board by the edges
- Avoid touching any components
- Store in ESD safe bag.

Avoid flexing the board.

3 Specification

3.1 Inputs

3.1.1 Signal (J5)

Input:	50 Ohms
Bandwidth:	30 MHz to 1700 MHz nominal
Level (Range1):	± 410 mV nominal
Level (Range2):	± 300 mV nominal

Range selectable via FPGA and ADC serial port; bandwidth limited by input transmission-line transformer. ADC 3dB bandwidth is 3GHz.

Note:
exceeding the maximum limit may result in permanent degradation of converter performance.

3.1.2 Clock In (J3)

Input:	50 Ohms, ac coupled
Level:	± 500 mV nominal. ± 200 mV minimum to +/1V maximum
Clock Rate:	500 MHz to 1700 MHz (doubled internally by the ADC)

Note:
exceeding the maximum voltage limit may result in permanent degradation of converter performance.

3.2 Input /Output

3.2.1 Clock Out (J2)

Impedance:	50 Ohms
Level:	± 400 mV nominal.
Source:	GTP or User Clock from XRC board.
Clock Rate:	20 MHz to 500 MHz, User Clock 300 MHz to 1500 MHz GTP

3.2.2 Aux IO Port (J1)

User configurable as input or output

Input:	4k7 Ohms, dc coupled
Level:	+3V3 LVTTL

3.2.3 GPIO Ports (J6 and J7)

User configurable as input or output, direct to FPGA pins.

Input:	dc coupled
Level:	2V5 logic

Note:
signals on these connectors must be restricted to 2V5 logic levels else damage may result.

4 Options

4.1 Connector type

- SMA (7 mm, standard)
- Long Barrel SMA (20 mm)
- SMB
- SMC

4.2 Order Code

XRM2-ADC-S4/3G -[Connector option] -[IO voltage option]

Fields in square brackets may be omitted in order to obtain the standard configuration for that option. For custom filter designs or other customisation requirements (e.g. connectors) please contact Alpha Data.

5 Related Documents

TBD

6 Design Examples

Example UCF, HDL files and Application software are available from Alpha Data for purchasers of this card.

Note:
This product requires an export licences for companies outwith EU, Australia, Canada, Japan, New Zealand, Norway, Switzerland or the USA. Contact the factory for further information.

7 Pinouts

Note:
V6/V7/K7/KU/VU Pinouts required

8 Board Layout

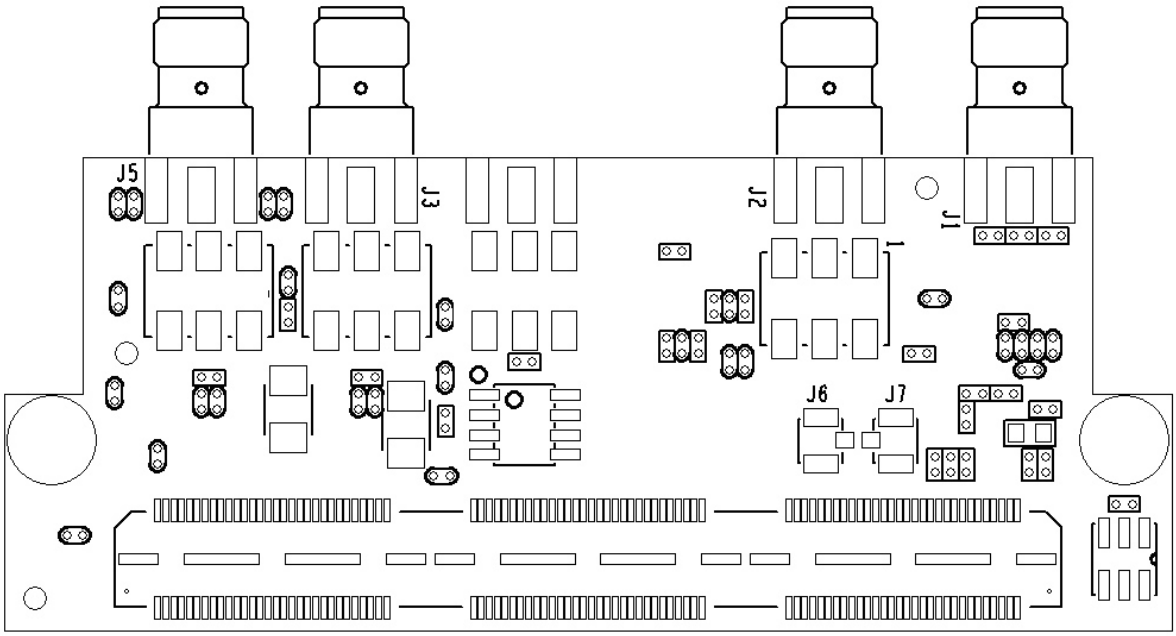

Figure 3 : XRM2-ADC-S4/3G Board Layout

J7 - Synch port

J6 - Synch port

J5 - ADC signal in

J3 - ADC Clock in

J2 - Clock out

J1 - Aux IO

Note:
This equipment generates, uses and can radiate electromagnetic energy. It may cause or be susceptible to electromagnetic interference if not installed and used with adequate EMI protection for specific applications.

Revision History

Date	Revision	Nature of Change
Dec-2007	1.0	First issue
Feb09	1.1	Updated block diagram, board layout. Updated pin connections list.
Jan 2012	1.2	Converted to new document system
Feb 2016	1.3	XRM2 Version

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